# KHX11000D3UL/1G

## *1GB 128M x 64-Bit PC3-11000*
## *CL5 240-Pin DIMM*

## DESCRIPTION:

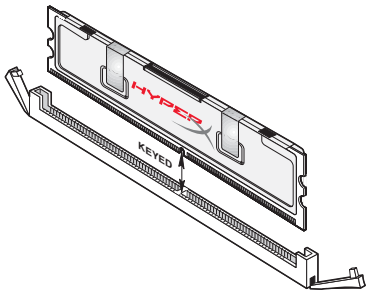
This document describes Kingston's 128M x 64-bit 1GB (1024MB) DDR3-1375 CL5 SDRAM (Synchronous DRAM) "ultra low latency" memory module, based on sixteen 64M x 8-bit DDR3 FBGA components. This module has been tested to run at DDR3-1375MHz at a low latency timing of 5-7-5 at 1.8V. The SPD is programmed to JEDEC standard latency DDR3-1333Mhz timing of 8-8-8 at 1.5V. This 240-pin DIMM uses gold contact fingers and requires +1.5V. The JEDEC standard electrical and mechanical specifications are as follows:

## FEATURES:

- ☑ JEDEC standard 1.5V ± 0.075V Power Supply
- ☑ VDDQ = 1.5V ± 0.075V
- ☑ 667MHz fCK for 1333Mb/sec/pin
- ☑ 8 independent internal bank
- ☑ Programmable CAS Latency: 5,6,7,8,9,10
- ☑ Posted CAS
- ☑ Programmable Additive Latency: 0, CL - 2, or CL - 1 clock
- ☑ Programmable CAS Write Latency(CWL) = 8(DDR3-1333)
- ☑ 8-bit pre-fetch
- ☑ Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with tCCD = 4 which does not allow seamless read or write [either on the fly using A12 or MRS]
- ☑ Bi-directional Differential Data Strobe
- ☑ Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- ☑ On Die Termination using ODT pin
- ☑ Average Refresh Period 7.8us at lower then TCASE 85°C, 3.9us at 85°C < TCASE . 95°C
- ☑ Asynchronous Reset
- ☑ 1333Mbps CL8 doesn’t have backward compatibility with 800Mbps CL5
- ☑ PCB : Height 1.180” (30.00mm), double sided component

## PERFORMANCE:

| | |
|---|---|
| ☑ CL(IDD) | 8 cycles |
| ☑ Row Cycle Time (tRCmin) | 48ns (min.) |
| ☑ Refresh to Active/Refresh Command Time (tRFCmin) | 90ns |
| ☑ Row Active Time (tRASmin) | 36ns (min.) |
| ☑ Power | TBD W (operating) |
| ☑ UL Rating | 94 V - 0 |
| ☑ Operating Temperature | 0° C to 85° C |
| ☑ Storage Temperature | -55° C to +100° C |




Preliminary

## MODULE DIMENSIONS: