

KHX6400D2UL/512

512MB 64M x 64-Bit PC2-6400

CL3 240-Pin DIMM

DESCRIPTION:

This document describes Kingston's ultra low-latency 64M x 64-bit (512MB) DDR2-800 CL3 SDRAM (Synchronous DRAM) memory module, based on eight 64M x 8-bit DDR2 FBGA components. This module has been tested to run at DDR2 800MHz at low latency timing of 3-3-3-10 at 2.3-2.35V. The SPD is programmed to JEDEC standard latency 800Mhz timing of 5-5-5-15 at 1.8V. This 240-pin DIMM uses gold contact fingers and requires +1.8V. The electrical and mechanical specifications are as follows:

FEATURES:

- ✓ Power supply : Vdd: 1.8V $\pm$ 0.1V, Vddq: 1.8V $\pm$ 0.1V
- ✓ Double-data-rate architecture; two data transfers per clock cycle
- ✓ Bidirectional data strobe(DQS)
- ✓ Differential clock inputs (CK and CK)
- ✓ DLL aligns DQ and DQS transition with CK transition
- ✓ Programmable Read latency 3, 4, 5 (clock)
- ✓ Burst Length: 4, 8 (Interleave/nibble sequential)
- ✓ Programmable Burst type (sequential & interleave)
- ✓ Timing Reference: 800MHz 5-5-5-15 at +1.8V / 800MHz 3-3-3-10 at +2.3-2.35V
- ✓ Edge aligned data output, center aligned data input
- ✓ Auto & Self refresh, 7.8 μ s refresh interval (8K/64ms refresh)
- ✓ Serial presence detect with EEPROM
- ✓ High Performance Heat Spreader
- ✓ PCB : Height 1.180" (30.00mm), single sided component

PERFORMANCE:

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|---|-------------------------------|
| ✓ Clock Cycle Time (tCK) CL=5 | 2.5ns (min.) / 8ns (max.) |
| ✓ Row Cycle Time (tRC) | 57.5ns (min.) |
| ✓ Refresh to Active/Refresh Command Time (tRFC) | 105ns |
| ✓ Row Active Time (tRAS) | 45ns (min.) / 70,000ns (max.) |
| ✓ Single Power Supply of | +1.8V (+/- .1V) |
| ✓ Power | 1.224 W (operating) |
| ✓ UL Rating | 94 V - 0 |
| ✓ Operating Temperature | 0° C to 55° C |
| ✓ Storage Temperature | -55° C to +125° C |



