

KHX8500S3ULK2/4GX

4GB (2GB 256M x 64-Bit x 2 pcs.)

PC3-8500 CL5 204-Pin SODIMM Kit

DESCRIPTION:

Kingston's KHX8500S3ULK2/4GX is a kit of two 256M x 64-bit 2GB (2048MB) PC3-8500 CL5 SDRAM (Synchronous DRAM) memory modules. Each module is based on sixteen 128M x 8-bit DDR3 FBGA components. Total kit capacity is 4GB (4096MB). Each module pair has been tested to run at DDR3- 1066MHz at an ultra-low latency timing of 5-5-5-15 at 1.5V. The SPDs are programmed to JEDEC standard latency 1066Mhz timing of 7-7-7 at 1.5V. Each 204-pin SODIMM uses gold contact fingers and requires +1.5V. The electrical and mechanical specifications are as follows:

FEATURES:

- ✓ JEDEC standard 1.5V $\pm$ 0.075V Power Supply
- ✓ VDDQ = 1.5V $\pm$ 0.075V
- ✓ 533MHz fCK for 1066Mb/sec/pin
- ✓ 8 independent internal bank
- ✓ Programmable CAS Latency: 5,6,7,8
- ✓ Posted CAS
- ✓ Programmable Additive Latency: 0, CL - 2, or CL - 1 clock
- ✓ Programmable CAS Write Latency(CWL) = 6(DDR3-1066)
- ✓ 8-bit pre-fetch
- ✓ Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either on the fly using A12 or MRS]
- ✓ Bi-directional Differential Data Strobe
- ✓ Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm $\pm$ 1%)
- ✓ On Die Termination using ODT pin
- ✓ Average Refresh Period 7.8us at lower then TCASE 85°C, 3.9us at 85°C < TCASE . 95°C
- ✓ Asynchronous Reset
- ✓ PCB : Height 1.180" (30.00mm), double sided component

PERFORMANCE:

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| ✓ CL(IDD) | 7 cycles |
| ✓ Row Cycle Time (tRCmin) | 50.63ns (min.) |
| ✓ Refresh to Active/Refresh Command Time (tRFCmin) | 110ns |
| ✓ Row Active Time (tRASmin) | 37.5ns (min.) |
| ✓ Power | 1.320 W (operating per module) |
| ✓ UL Rating | 94 V - 0 |
| ✓ Operating Temperature | 0° C to 85° C |
| ✓ Storage Temperature | -55° C to +100° C |



